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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,564	BARRY ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 14-29 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE as received on 1/12/2005.

Claim Objections

3. Claim 25 is objected to because of the following informalities: Please insert --is-- before "configuration" in line 2. Appropriate correction is required.

Withdrawn Rejections

4. Applicant, by way of amendment, has overcome the prior art rejections set forth in the previous Office Action for claims 14-29. Consequently, these rejections are hereby withdrawn by the examiner. However, upon further consideration, a new ground(s) of rejection is applied below to at least a portion of the claims.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 24-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 24 recites the limitation "the S/P bit" in the 3rd to last line. There is insufficient antecedent basis for this limitation in the claim. For purposes of examination, the examiner will assume applicant meant to claim "the SP/PE bit".

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 14-15 and 19-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al., U.S. Patent No. 5,542,074 (herein referred to as Kim).

10. Referring to claim 14, Kim has taught an array processor comprising:

a) a physical MxN array organization of at least two processing elements. See Fig.1 components PE $12_{1,2,\ldots,N}$. This array of elements is at least N rows and 1 column, or an Nx1 array organization.

b) a processor state register storing a context status bit (CSB), the CSB having a first state and a second state, each processing element operating to detect the state of the CSB. See Fig.2, component 68 (EP register) and column 8, lines 10-22.

c) the array processor upon detection of the first state of the CSB operating in a first operating context adapted for processing a first software task where the first software task is written for an MxN array organization which matches the physical MxN array organization, where M represents the number of rows of processing elements and N represents the number of columns of processing elements. Looking at Fig.1, when each of the processing elements is enabled, the task is executed on the MxN array configuration (i.e., the Nx1 configuration shown in Fig.1).

d) the array processor upon detection of the second state of the CSB operating in a second operating context adapted for a second software task where the second software task is written for a second array processor having an OxP operating configuration where O is the number of rows of processing elements and P is the number of columns of processing elements, the OxP operating configuration not matching the physical MxN array organization as either M≠O, N≠P, or N≠O and N≠P. See Fig.1, and note that if all but the last processing element is enabled, then the task would be executed on an OxP configuration (i.e., the (N-1)x1 configuration). That is, there would be one less row in the array (N-1). So, M≠O, where M=N, and O=N-1.

11. Referring to claim 15, Kim has taught an array processor as described in claim 14. Kim has further taught that in the first operating context, the array processor utilizes a first and a second set of register files, the first set of register files associated with one of the processing elements and the second set of register files associated with another of the processing elements. See Fig.1 and Fig.2, component 46. Each processing element has its own register file, and if that element is enabled, then that register file will be used during processing.

12. Referring to claim 19, Kim has taught a method for providing reconfiguration of a first array processor having a physical MxN array organization to emulate operation of a second array

processor having a physical OxP array organization where M and O represent the number of rows of processing elements and N and P represent the number of columns of processing elements, the method comprising:

a) providing the first array processor having at least two processor elements arranged in the physical MxN array organization. See Fig.1 components PE $12_{1,2,\ldots,N}$. This array of elements is at least N rows and 1 column, or an Nx1 array organization.

b) storing a context status bit (CSB), the CSB having a first state and a second state. See Fig.2, component 68 (EP register) and column 8, lines 10-22.

c) detecting the state of the CSB. See Fig.2, component 68 (EP register) and column 8, lines 10-22.

d) upon detection of the first state, operating in a first operating context adapted for processing a first software task, wherein the first software task is written for the physical MxN array organization. Looking at Fig.1, when each of the processing elements is enabled, the task is executed on the MxN array configuration (i.e., the Nx1 configuration shown in Fig.1).

d) upon detection of the second state, operating in the second operating context adapted for processing a second software task, wherein the second software task is written for the physical OxP array configuration, where either $M \neq O$ or $N \neq P$. See Fig.1, and note that if all but the last processing element is enabled, then the task would be executed on an OxP configuration (i.e., the (N-1)x1 configuration). That is, there would be one less row in the array (N-1). So, $M \neq O$, where M=N, and O=N-1.

13. Referring to claim 20, Kim has taught a method as described in claim 19. Kim has further taught that the operating in the second operating context step further comprises setting the

CSB to the first state and returning to the first operating context. It should be realized that elements may be enable and disabled throughout system execution. Consequently, when all units are once again enabled, the first context is once again achieved.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 16-17 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Dowling, U.S. Patent No. 6,128,728 (as applied in the previous Office Action).

16. Referring to claim 16, Kim has taught an array processor as described in claim 15. Kim has not explicitly taught an eventpoint mechanism to trigger storing the data contents of the first set of register files in the background while the first software task uses the second set of register files in the foreground. However, Dowling has taught such a concept. See column 4, lines 32-46, and column 5, line 14, to column 6, line 6. With such a scheme, the inactive register set would be stored in the background while the active register set would be manipulated by a processor in the foreground. This would maximize the efficiency by making use of otherwise unused external memory cycles, as disclosed in the abstract. That is, when a processor is not accessing memory, the contents of the inactive register file may be stored in the background during those unused memory cycles. Therefore, in order to increase efficiency, it would have been obvious to one of ordinary skill in the art at the time of the invention to store the contents of

a first register set to memory in the background while a task is uses a second register set in the foreground.

17. Referring to claim 17, Kim has taught an array processor as described in claim 15. Kim has not explicitly taught an eventpoint mechanism to trigger loading the first set of register files in the background while the first software task uses the second set of register files in the foreground. However, Dowling has taught such a concept. See column 4, lines 32-46, and column 5, line 14, to column 6, line 6. With such a scheme, the inactive register set would be loaded in the background while the active register set would be manipulated by a processor in the foreground. This would maximize the efficiency by making use of otherwise unused external memory cycles, as disclosed in the abstract. That is, when a processor is not accessing memory, the inactive register file may be loaded in the background during those unused memory cycles. Therefore, in order to increase efficiency, it would have been obvious to one of ordinary skill in the art at the time of the invention to restore a first register set from memory in the background while a task is using a second register set in the foreground.

18. Referring to claim 21, Kim has taught a method as described in claim 19. Kim has further taught that the physical MxN array organization comprises a 1x1 layout and the emulated physical OxP array organization comprises a 1x0 layout, wherein the 1x0 layout defines a sequence processor (SP) executing sequential instructions. See Fig.1. The OxP array would include PEs 12_1 being enabled. That is, there'd be an SP executing instructions. If a next PE is then enabled (PE 12_2), then a 1x1 array would be achieved (1 row and 1 column of PEs would be added to the already enabled SP).

19. Referring to claim 22, Kim has taught a method as described in claim 19. Kim has further taught that the physical MxN array organization comprises a 1x2 layout and the emulated physical OxP array organization comprises a 1x1 layout. See Fig.1, and note that when only PE 12_1 is enabled, a 1x1 array is achieved (1 row, 1 column of PEs). If a next PE (PE 12_2) is then enabled, a 1x2 array would be created (there's be 1 row, and 2 columns).

20. Referring to claim 23, Kim has taught a method as described in claim 19. Kim has further taught that the physical MxN array configuration comprises a 1x5 layout and the emulated physical OxP array configuration comprises a 2x2 layout. See Fig.1, and note that when 5 PEs are enabled, a 1x5 array is achieved (1 row, 5 columns of PEs). If one of the 5 enabled PEs is disabled, then a 2x2 array would be generated (i.e., there'd be 4 PEs enabled). It should be noted that applicant does not claim that there would be 2 rows and 2 columns of elements. Instead, the configuration comprises a 2x2 layout, or as interpreted, a 4-element layout.

21. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Sims, U.S. Patent No. 6,088,510.

22. Referring to claim 18, Kim has taught an array processor as described in claim 14. Kim has not taught that each processing element of the at least two processing elements has a physical identifier and a virtual identifier, wherein during the processing of the first software task, instructions are operable in each processing element according to its physical identifier, wherein during the processing of the second software task, instructions are operable in each processing element according to its virtual identifier. However, Sims has taught that in a group of

processing elements having physical identifiers, some may simulate virtual processing elements having virtual identifiers. See Fig.1, components 13, and column 6, lines 21-43. Virtual processors are advantageous because they allow multiple instruction streams to be executed. So, if a particular physical element is associated with multiple virtual processors, then that physical element is able to execute multiple streams of instructions concurrently. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kim such that virtual processors with virtual identifiers are implemented. And, it is already known that Kim can enable/disable any number of the processing elements. Therefore, a first task will use a first number of physical elements having physical IDs while a second task will use a second number of physical elements which are associated with virtual elements having virtual elements.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
March 22, 2006

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